

REMARKS

Claims 32-53 and 58-61 are pending, with claims 32, 36, 38, 42, 44, 45, 47, 48, 58, and 61 being in independent form. Claims 34, 38, 40, and 44 are amended, and claims 54-57 are canceled without prejudice or disclaimer.

Applicant notes the Examiner's acknowledgment of Applicant's election of Group 1, claims 32-53 and 58-61. Claims 54-57 drawn to the non-elected invention are canceled, accordingly. Applicant reserves the right to file a divisional application with claims directed toward the subject matter of the canceled claims at a later date.

Applicant acknowledges with appreciation the Examiner's indication of the allowability of claims 36-37, 39, 41, 45, 47-49, 51, 53 and 61. Applicant also notes the Examiner's indication of the allowability of claims 38, 40, 50, and 52 if suitably amended.

In the Office Action, claims 34, 38, 40, 42-44 and 46 stand rejected for indefiniteness.

Applicants have amended claims 34, 40, and 48 to remove the language objected to in the Action.

With respect to claim 42, Applicant draws the Examiner's attention to FIG. 3 depicting a differential band-pass charge sampling circuit. In particular, FIG. 3 illustrates first and a second band-pass charge sampling (BPCS) circuits. The first BPCS circuit is depicted in the top half of the figure (including elements 2A, 2B, 6A, and 3A), and the second BPCS circuit is depicted in the bottom half of the figure (including elements 2C, 2D, 6B, and 3B).

As illustrated, the second BPCS circuit is a mirror image of the first BPCS circuit. Moreover, the first BPCS circuit has a first signal input 2A and a second signal input 2B. In addition, the second BPCS circuit has a first signal input 2D (which is coupled to the second input of the first sampling circuit 2A) and a second signal input 2C (which is coupled to the first input of the first sampling circuit 2B). Accordingly, Applicant respectfully asserts that claim 42 particularly points out and distinctly claims the subject matter which the Applicant regards as the invention.

With respect to claim 44, Applicant has amended this claim to correct a typographical error that occurred when replacing the original claims of the application to better conform to U.S. practice. Claim 44 redefines the subject matter of originally filed claim 13, which clearly recites a common control signal generator. As such,

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Applicant asserts that the scope of claim 44 has not been narrowed, or even changed, by this amendment. Accordingly, those seeking to interpret the claim should not limit it only to its literal scope.

In view of the above, Applicant respectfully asserts that the pending claims are now sufficiently definite, and requests the Examiner to reconsider and withdraw the indefiniteness rejections raised in the Action.

Claims 32-35 and 58-60 stand rejected for anticipation by U.S. Patent No. 5,281,860 to Krenik et al. ("Krenik"). Also, claims 32, 34-35 and 58-60 stand rejected for anticipation by U.S. Patent No. 6,181,748 to Lin et al. ("Lin"). Applicant believes these claims to be novel and inventive over the documents cited in the Action for the following reasons.

Anticipation requires that every feature of the claimed invention be shown in a single prior document. In re Paulsen, 30 F.3d 1475 (Fed. Cir. 1994); In re Robertson, 169 F.3d 743 (Fed. Cir. 1999). The pending claims positively recite limitations that are not disclosed (nor suggested) in the cited document.

For example, claim 32 recites, among other things, "an integrator for integrating the analog input signal during a sampling phase." Similarly, method claim 58 recites "integrating an analog input signal during a sampling phase." Krenik does not describe or suggest these related features, and thus is insufficient to support the anticipation rejection.

The Action asserts that the integrated circuit shown in FIG. 6 of Krenik anticipates the claimed charge sampling circuit, but this assertion cannot be true. Krenik describes on column 6, lines 20-31, in connection with FIG. 6, an integrated circuit (IC) that first receives analog inputs from multiple channels, and then samples these inputs onto an input integrator. Krenik further describes that the IC samples these integrated values onto the switched capacitor multiplexer capacitors for each channel. Krenik then states that the sampling phase is ended and, only then, does the circuitry transmit the sampled value for each channel onto the output integrator amplifier capacitor (column 6, lines 22-29).

Thus, Krenik discloses an integrated circuit in which integration of the sampled data occurs after the sampling phase has ended. Moreover, as made clear in FIG. 5, which shows a waveform diagram of the switch-timing disclosed in Krenik, S₃ (that controls the passing of sampled data to the integrator 27) and S₄ (that controls the

sampling of the input data onto the capacitor C₂) are never active at the same time, making the integration of the signal during the sampling phase impossible. Indeed, Krenik's arrangement is precisely the conventional voltage sampling arrangement used for analog-to-digital conversion that Applicant discusses in the background section of this application and is seeking to improve upon.

In contrast, the present invention, as defined by claims 32 and 58, defines a circuit and method whereby the analog signal is integrated during the sampling phase. Accordingly, Applicant believes claims 32 and 58, and the claims that depend from these claims, to be novel and inventive over Krenik for at least this reason.

Claims 32, 34-35 and 58-60 also stand rejected for anticipation over Lin under § 102(b) of the patent statute. Applicant notes that while Lin has a U.S. filing date of July 7, 1998, Lin was not published until the patent issued on January 30, 2001. This application has an effective filing date of September 28, 1999. Accordingly, Lin does not qualify as prior art under § 102(b), but rather can qualify as prior art only under § 102(e).

Notwithstanding the above, like Krenik, Lin is insufficient to sustain the anticipation rejection because Lin does not describe or suggest all of the features defined in the rejected claims. For example, the Action asserts that Lin anticipates the claimed invention because Lin describes "a control signal generator for controlling an analog input signal to the charge sampling circuit," but this assertion is not correct. In contrast, Lin describes a pulse shaper that converts a digital input signal (D0 and D1) to a five staircase-type analog waveform by using a fully differential switched-capacitor integrator (see Abstract). Because Lin describes a charge sampling circuit that converts a digital input signal to an analog signal, Lin fundamentally differs from the rejected claims, which are directed to versatile charge sampling circuits used for analog-to-digital conversion.

Moreover, Lin does not describe "an integrator for integrating the analog input signal," as recited in claim 32, nor does Lin describe a method comprising the step of "integrating an analog input signal," as recited in claim 58. To the contrary, Lin describes a fully differential switched-capacitor integrator (40) for integrating a digital input signal D0 and D1 (column 3, lines 8-12).

Even if the Action were to assert that the described VINTP and VINTN signals are analog input signals within the scope of claims 32 and 58, Lin still does not

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disclose "an integrator for integrating the analog input signal during a sampling phase." Rather, the Sampled-Hold circuit (5) described in Lin filters the unwanted spike signal, which is generated by the fully differential switched-capacitor integrator, after the integration phase has been completed (column 5, lines 1-4). As shown in FIG. 5(b), the control clock signals CLK22 and CLK23 for controlling the Sampled-Hold circuit never overlap. As a result, integration during a sampling phase, according to the method and apparatus described in Lin, is not possible. Therefore, Lin not only fails to describe integrating the analog input signal during a sampling phase, but Lin does not even suggest this feature.

For at least the reasons discussed above, neither Krenik nor Lin can anticipate the novel charge sampling circuit as defined by claims 32 and 58. Neither Krenik nor Lin describe or suggest a charge sampling circuit comprising an integrator for integrating an analog input signal during a sampling phase. Further, Lin does not even describe an integrator for integrating an analog input signal. Accordingly, these claims, and the claims that depend from them, are novel and inventive over what is described in either Krenik or Lin for at least these reasons.

For the foregoing reasons, Applicant believes the application to be in condition for allowance, and respectfully requests notice thereof at an early date. The Examiner is encouraged to telephone the undersigned at the below-listed number if, in the Examiner's opinion, such a call would aid in the examination of this application.

Respectfully submitted,

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ATTACHMENT TO AMENDMENT DATED JULY 26, 2002

Marked-Up Copy of Amended Claims

34. (Amended) The charge sampling circuit according to claim 32, wherein the control signal generator [is adapted to control] controls the integrator to hold the sample until a resetting signal from the generator is applied to a control input of the integrator.

38. (Amended) A band-pass charge sampling circuit, comprising:
a control signal generator for controlling a first and second portion of a differential analog signal;
a first signal input for receiving the first portion of the differential analog signal;
a second signal input for receiving the second portion of the differential analog signal;

an integrator; and

a weighting-and-sampling element for processing the differential analog signal during a weighting-and-sampling phase responsive to a weighting-and-sampling signal from said control signal generator, wherein a current of said differential analog signal passes through said weighting-and-sampling element only when said weighting-and-sampling signal is in a weighting-and-sampling phase, said control signal generator [is adapted] for controlling an output signal of said weighting-and-sampling element to be integrated by the integrator during said weighting-and-sampling phase, and a current of the output signal of said weighting-and-sampling element is integrated to an integrated charge for producing one of a proportional voltage sample and a proportional current sample at a signal output upon completion of said weighting-and-sampling phase.

40. (Amended) The band-pass charge sampling circuit according to claim 38, wherein the control signal generator [is adapted to control] controls the integrator to hold the sample until a resetting phase controlled by said resetting signal begins.

44. (Amended) A parallel charge sampling circuit, comprising:
a common control signal generator; and

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a plurality of charge sampling circuits, each respective charge sampling circuit having[.]

a first analog input being a signal input of the respective charge sampling circuit and responsive to a controlling signal from the common control signal generator; and

[a control signal generator for controlling an analog input signal to the charge sampling circuit; and]

an integrator for integrating the analog input signal during a sampling phase responsive to a sampling signal from the common control signal generator[.]:

wherein all analog first signal inputs are connected together as a common analog signal input of said parallel charge sampling circuit, [all control signal generators of said charge sampling circuits are replaced by a common control signal generator,] a multiplexer having a plurality of signal inputs connected to the signal outputs of said charge sampling circuits respectively, control inputs connected to multiplexing signal outputs of said common control signal generator, and a signal output for multiplexing the outputs of said charge sampling circuits to the output of said parallel charge sampling circuit when the outputs of said charge sampling circuits are in holding phases.

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